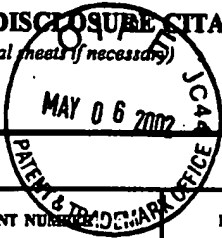


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Docket Number (Optional)

BUR920020023 US1

Application Number

10/063,142

Applicant(s)

Timothy Lehner, et al.

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03/25/02

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JH		5,481,484	01/02/96	Ogawa et al.	/	/	
		5,535,146	07/09/96	Huang et al.	/	/	
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JH		6,005,829	12/21/99	Conn	/	/	

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

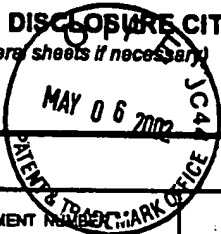
JH	Bina Ackalloor, Dinesh Galtonde, "An Overview of Library Characterization in Semi-Custom Design" 5/97 IEEE 1998 Custom Integrated Circuits Conference, pp. 305-312
JH	Jerry D. Hayes and Larry Wissel, "Behavioral Modeling for Timing, Noise, and Signal Integrity Analysis" IBM Microelectronics Division

EXAMINER	DATE CONSIDERED
<i>[Signature]</i>	8/4/2005

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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JYP		Chandrakasan et al., "Design of High-Performance Microprocessor Circuits" ISBN 0-7803-6001-X, IEEE Order No. PC5836, Chapter 16.3 pp. 338-345
JYP		Jessica Qian, et al., "Modelling the 'Effective Capacitance' for the RC Interconnect of CMOS Gates" December 1994, Volume 13, No. 12, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems pp. 1526-1535

EXAMINER	DATE CONSIDERED
	8/4/2005

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